

EXAMINER'S AMENDMENT

1. An examiner's amendment to the record appears below. Should the changes and/or additions be unacceptable to applicant, an amendment may be filed as provided by 37 CFR 1.312. To ensure consideration of such an amendment, it MUST be submitted no later than the payment of the issue fee.

Authorization for this examiner's amendment was given in a telephone interview with Larry N. Anagnos on 04 august 2008.

The application has been amended as follows:

1.) Claim 13 is cancelled.

REASONS FOR ALLOWANCE

2. The following is an examiner's statement of reasons for allowance: The instant application discloses a digital-control type clock data recover circuit. A search of prior art records has failed to teach or suggest, alone or in combination:

a digital control-type clock data recovery circuit comprising:
“a multistage register circuit storing onset of said DOWN signal and onset of said UP signal at each of comparing opportunities during a phase detection period corresponding to a plurality of cycles of said data recovery clock signal, generating an OUT DOWN signal if at least one DOWN signal is stored at an end of the phase detection period and generating an OUT UP signal if at least one UP signal is stored at the end of the phase detection period; and a clock-phase generation unit generating said data recovery clock signal and shifting the phase of said data recovery clock signal on the basis of the OUT UP signal and the OUT DOWN signal output from said multistage register circuit so as to separate edges of said data recovery clock signal away from edges of said input data by a predetermined time gap” as disclosed in claim 3.

“a digital control-type clock data recovery circuit:

“ wherein said function to track a wander of input data by comparing a position of an edge of said input data with a position of an edge of a clock signal is executed under a condition expressed by a relation given as follows:

$$B \times \sin(2\pi r \times T_a/T_w) \geq T/N$$

where symbol B denotes a maximum phase change of said input data over a period of time, symbol T_a denotes a loop delay, which is a period of time between an output operation carried out by a counter and a first phase comparison, symbol T_w denotes a phase deviation period, symbol T denotes a clock period, symbol N denotes the number of phase divisions, where N is a finite number, and T/N denotes a difference between 2 adjacent phases determined by said number of phase divisions N” as disclosed in claim 10.

Any comments considered necessary by applicant must be submitted no later than the payment of the issue fee and, to avoid processing delays, should preferably accompany the issue fee. Such submissions should be clearly labeled “Comments on Statement of Reasons for Allowance.”

CONCLUSION

3. Any inquiry concerning this communication or earlier communications from the examiner should be directed to Lawrence B Williams whose telephone number is 571-272-3037. The examiner can normally be reached on Monday-Friday (8:00-6:00).

If attempts to reach the examiner by telephone are unsuccessful, the examiner’s supervisor, Ghayour Mohammad can be reached on 571-272-3021. The fax phone number for the organization where this application or proceeding is assigned is 571-273-8300.

Information regarding the status of an application may be obtained from the Patent Application Information Retrieval (PAIR) system. Status information for published applications may be obtained from either Private PAIR or Public PAIR. Status information for unpublished applications is available through Private PAIR only. For more information about the PAIR system, see <http://pair-direct.uspto.gov>. Should you have questions on access to the Private PAIR system, contact the Electronic Business Center (EBC) at 866-217-9197 (toll-free).

lbw
August 22, 2008

/Lawrence B Williams/

Primary Examiner, Art Unit 2611

/Mohammad H Ghayour/

Supervisory Patent Examiner, Art Unit 2611